AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A power amplifier circuit comprising:

a first amplifier having a first subsection and a second subsection, the first amplifier configured to receive an input signal, and in response, provide a first path output signal;

a first delay circuit configured to introduce a first delay to the input signal, thereby creating a second path delayed input signal;

a second amplifier having a first subsection and a second subsection, the second amplifier configured to receive the second path delayed input signal, and in response, provide a ~~first~~ second path delayed output signal, wherein the first subsection is enabled;

an impedance inverter circuit configured to provide impedance inversion and introduce a ~~second~~ first path delay to the first path output signal, thereby creating a ~~second~~ first path delayed output signal;

a node connecting an output of the impedance ~~inversion~~ inverter and an output of the second amplifier, the node configured to combine the first path and second path delayed output signals, thereby creating an amplified output signal; and

a bias control circuit configured to provide a first bias voltage that enables the first subsection of the first amplifier and the first subsection of the second amplifier, to causes ~~the first amplifier~~ the enabled subsections to operate in a linear mode ~~when the first amplifier is enabled~~ during a low power mode, wherein the second subsection of the first amplifier and the second subsection of the second amplifier are disabled in the low power mode, and a second bias voltage that enables the second subsection of the first amplifier and the second subsection of the second amplifier, , wherein the first subsection of the first amplifier and the first subsection of the second amplifier are enabled in the high

power mode, to causes the ~~second~~ enabled amplifier subsections to operate in a linear mode ~~when the second amplifier is enabled~~ during a high power mode.

2. (Currently Amended) The power amplifier of claim 1, wherein the bias control circuit comprises:

means for activating the first bias voltage and deactivating the second bias voltage when a control signal identifies ~~a~~ the low power mode; and

means for activating both the first and second bias voltages when the control signal identifies ~~a~~ the high power mode.

3. (Canceled)

4. (Original) The power amplifier of claim 1, further comprising an impedance matching circuit, wherein the input signal is provided to the first amplifier and the delayed input signal is provided to the second amplifier through the impedance matching circuit.

5. (Original) The power amplifier of claim 4, further comprising an input amplifier stage, wherein the input signal is provided to the first amplifier and the delayed input signal is provided to the second amplifier through the input amplifier stage.

6. (Original) The power amplifier of claim 1, wherein the first delay circuit comprises an impedance inverter circuit.

7. (Original) The power amplifier of claim 6, wherein the first amplifier exhibits a first impedance optimum load, and the second amplifier exhibits a second impedance optimum load, and the impedance inverter circuit exhibits a characteristic impedance equal to the first impedance.

8. (Original) The power amplifier of claim 1, wherein the first delay is equal to the second delay.

9. (Original) The power amplifier of claim 1, wherein the first amplifier comprises a first set of transistors, and the second amplifier comprises a second set of transistors.

10. (Original) The power amplifier of claim 9, wherein the first set of transistors are coupled to receive the first bias voltage, and the second set of transistors are coupled to receive the second bias voltage.

11. (Original) The power amplifier of claim 9, wherein a first subset of the first set of transistors are coupled to receive the first bias voltage, a second subset of the first set of transistors are coupled to receive the second bias voltage, and the second set of transistors are coupled to receive the second bias voltage.

12. (Previously Presented) The power amplifier of claim 1, further comprising:

a third amplifier configured to receive an input signal, and in response, provide a second output signal; and

a third delay circuit configured to introduce the second delay to the second output signal, thereby creating a third delayed output signal;

wherein the means for combining combines the first, second and third delayed output signals, thereby creating the amplified output signal, and the bias control circuit is configured to provide a third bias voltage that causes the third amplifier operate in a linear mode when the third amplifier is enabled.

13. (Previously Presented) A method of amplifying an input signal, comprising:

providing the input signal to a first amplifier;

applying a first bias voltage to the first amplifier to enable the first amplifier and cause the first amplifier to operate in a linear mode, such that the first amplifier provides a first output signal in response to the input signal;

introducing a first delay to the input signal, thereby creating a delayed input signal;

providing the delayed input signal to a second amplifier;

applying a second bias voltage to the second amplifier to enable the second amplifier and cause the second amplifier to operate in a linear mode, wherein the second amplifier provides a first delayed output signal in response to the delayed input signal;

introducing a second delay to the first output signal, thereby creating a second delayed output signal; and

combining the first and second delayed output signals at an output node of the second amplifier, thereby creating an amplified output signal.

14. (Original) The method of claim 13, further comprising selecting the first delay to be equal to the second delay, such that the first and second delayed output signals are substantially in phase.

15. (Original) The method of claim 13, further comprising disabling the second amplifier in a low power mode.

16. (Original) The method of claim 13, further comprising introducing the second delay with an impedance inverter circuit.

17. (Original) The method of claim 16, further comprising selecting a characteristic impedance of the impedance inverter circuit to be equal to an optimum load impedance of the first amplifier.

18. (Original) The method of claim 13, further comprising:

providing the input signal to the first amplifier through an impedance matching circuit; and

providing the delayed input signal to the second amplifier through the impedance matching circuit.

19. (Original) The method of claim 18, further comprising:

providing the input signal to the first amplifier through an input amplifier stage; and

providing the delayed input signal to the second amplifier through the input amplifier stage.

20. (Original) The method of claim 13, wherein applying the first and second bias voltages to enable the first and second amplifiers comprise:

applying the first bias voltage to a first set of transistors in the first amplifier; and

applying the second bias voltage to a second set of transistors in the second amplifier.

21. (Original) The method of claim 20 further comprising applying the second bias voltage to a third set of transistors in the first amplifier to enable the first amplifier.

22. (Original) The method of claim 13, further comprising:

providing the input signal to a third amplifier;

enabling the third amplifier to operate in a linear mode, such that the third amplifier provides a third output signal in response to the input signal;

introducing a third delay to the third output signal, thereby creating a third delayed output signal; and

combining the first, second and third delayed output signals, thereby creating an amplified output signal.

23. (New) A power amplifier circuit comprising:

a first amplifier having a first subsection and a second subsection, the first amplifier configured to receive an input signal, and in response, provide a first path output signal;

a first delay circuit configured to introduce a first delay to the input signal, thereby creating a second path delayed input signal;

a second amplifier having a first subsection and a second subsection, the second amplifier configured to receive the second path delayed input signal, and in response, provide a second path delayed output signal, wherein the first subsection is enabled;

an impedance inverter circuit configured to provide impedance inversion and introduce a first path delay to the first path output signal, thereby creating a first path delayed output signal;

a node connecting an output of the impedance inverter and an output of the second amplifier, the node configured to combine the first path and second path delayed output signals, thereby creating an amplified output signal; and

a bias control circuit configured to enable the first subsection of the first amplifier stage, the second subsection of the first amplifier stage, and the first subsection of the second amplifier stage, to cause the enabled subsections operate in a linear mode during a low power operation, wherein the second subsection of the second amplifier stage is disabled in the low power operation, and a second bias voltage that enables the second subsection of the second amplifier stage during a high power operation, wherein all subsections are enabled in the high power operation, to cause the enabled amplifier stages to operate in a linear mode during the high power operation.